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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,872	04/12/2004	Katsuhiro Uesugi	67161-148	1856

7590 07/21/2005

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EXAMINER	
KRAIG, WILLIAM F	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,872	UESUGI ET AL.	
	Examiner	Art Unit	
	William Kraig	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/12/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Bost et al. (US Patent 5270256).

Regarding claim 1, Figs. 18 and 19 of Bost et al., shown below, disclose a semiconductor device comprising:

a semiconductor substrate (30) having a main surface (30a, 170);

a semiconductor element (located within region 45)(Bost et al., Col.5, Lines 5-8) formed on said main surface (30a, 170);

an interlayer insulating film (70,110) having a top surface (110a) and a peripheral edge (the edges of 70 and 110 as seen in gray in Figure 1 (drawn by the examiner), below) extending from said top surface (110a) to said main surface (30a, 170), and formed on said main surface (30a, 170) to cover (Bost et al., Col.5, Lines 12-15) said semiconductor element (located within region 45)(Bost et al., Col 5, Lines 5-8)), wherein in said interlayer insulating film (70,110), strip-like first (191a) and second (191b) groove portions are formed to be placed between said semiconductor element (located within region 45)(Bost et al., Col 5, Lines 5-8)) and said peripheral edge (the edges of 70 and 110 as

seen in gray in Figure 1(a combined view of Figs. 18 and 19 of Bost et al., showing an angled view of a corner of the die (40) shown in Fig. 19, and the cross section of the die shown in Fig. 18) (drawn by the examiner), below), to extend in parallel with said main surface (30a, 170) and to extend in a predetermined direction at a spacing (193) with each other, and a plurality of third groove portions (191c,191d) are formed to diverge from said first (191a) and second (191b) groove portions and to extend in a direction different from an extending direction of said first (191a) and second (191b) groove portions; and

a metal (171) filling said first (191a), second (191b) and third (191c,191d) groove portions.

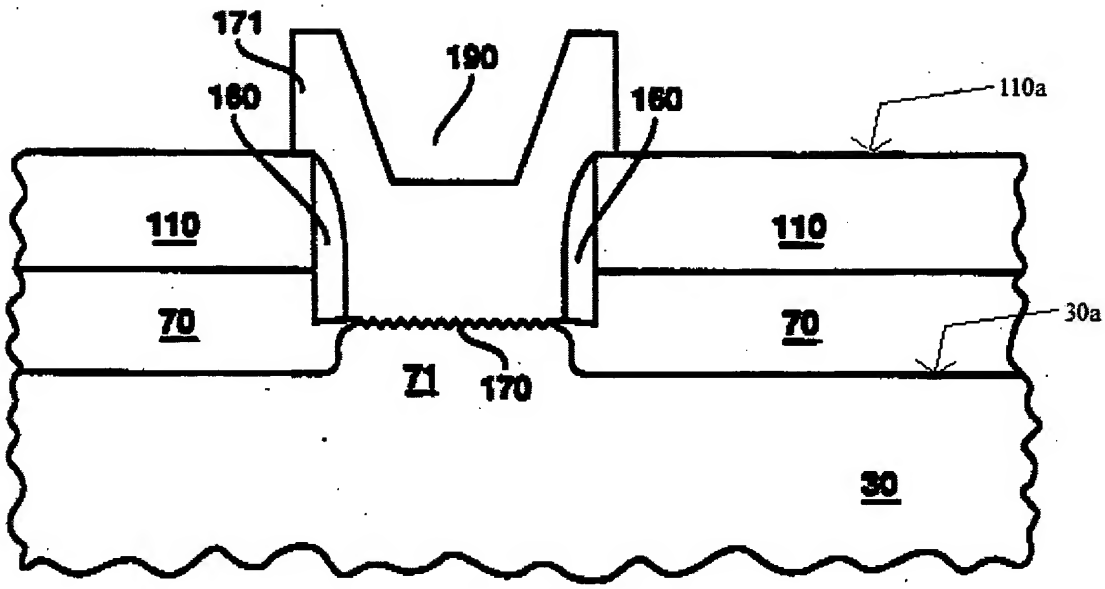

FIGURE 18

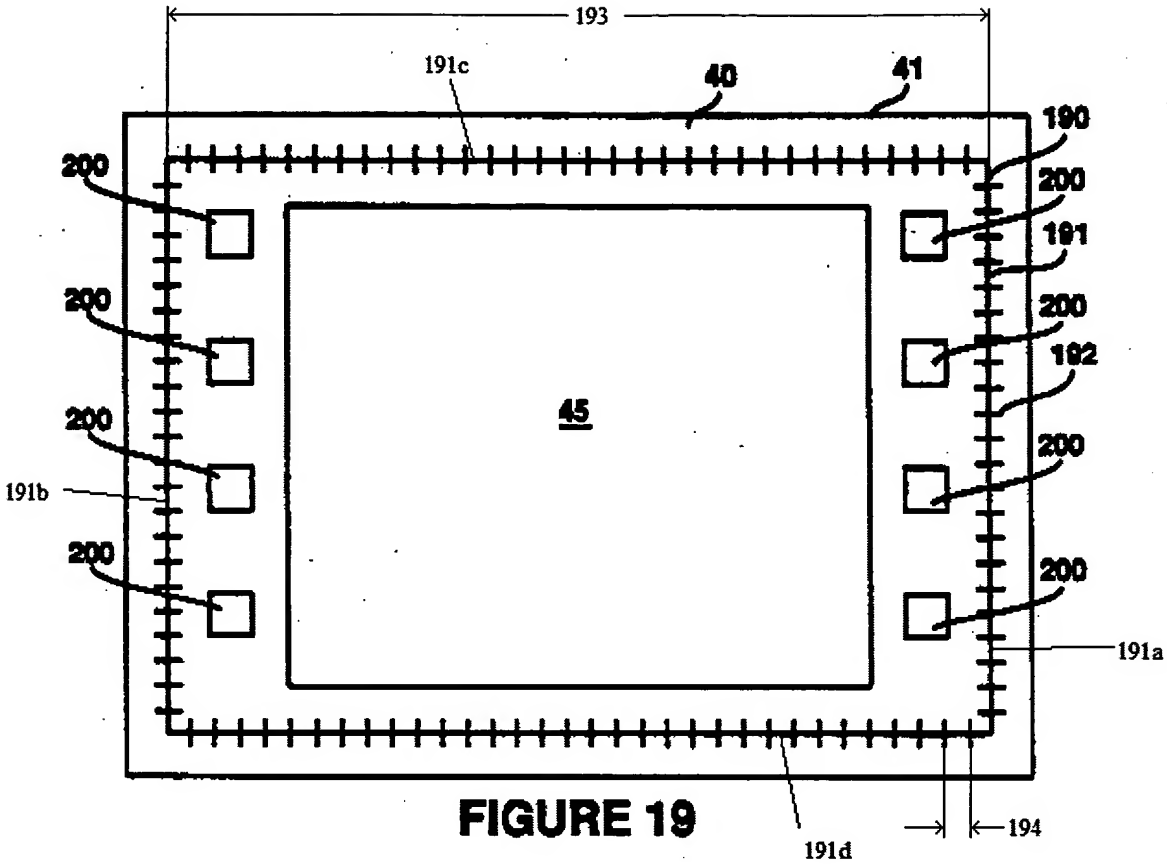
193
191c
40
41
190
200
200
191
200
200
192
45
200
200
191b
200
200
191a
191d
194

FIGURE 19

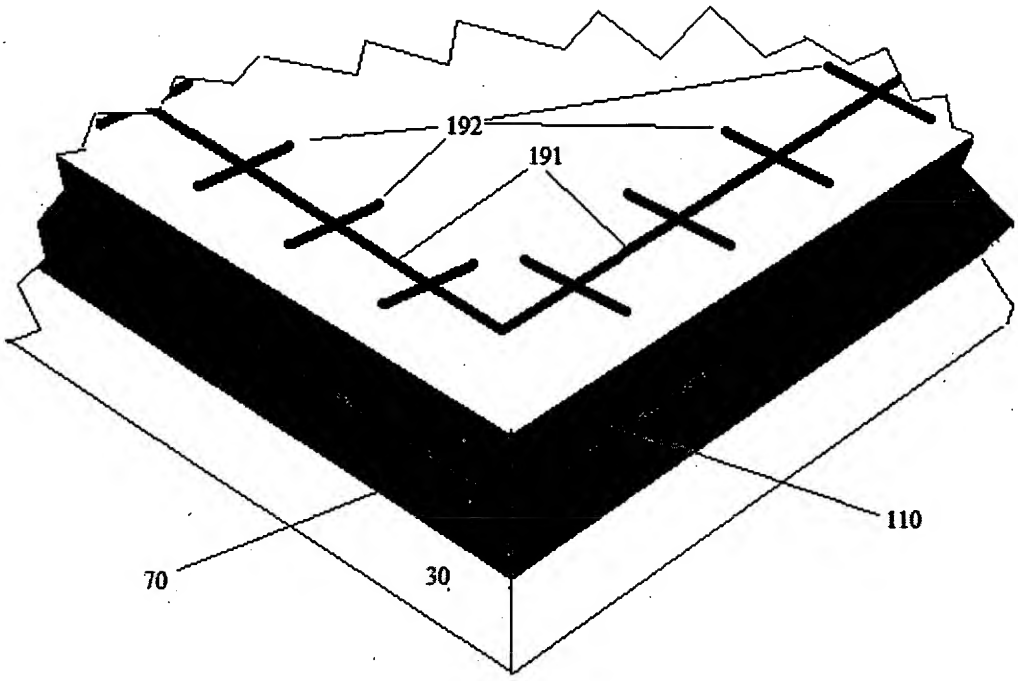

Figure 1

Regarding claim 2, Figs. 18 and 19 of Bost et al., shown above, disclose the semiconductor device of claim 1, wherein said third (191c,191d) groove portion is formed between said first (191a) groove portion and said second (191b) groove portion.

Regarding claim 3, Figs. 18 and 19 of Bost et al., shown above, disclose the semiconductor device of claim 1, wherein said third (191c,191d) groove portion links said first (191a) groove portion and said second (191b) groove portion.

Regarding claim 4, Figs. 18 and 19 of Bost et al., shown above, disclose the semiconductor device of claim 1, wherein said first (191a), second (191b) and third (191c,191d) groove portions reach said main surface (30a, 170) from said top surface (110a).

Regarding claim 5, Figs. 18 and 19 of Bost et al., shown above, disclose the semiconductor device of claim 1, wherein said first (191a) and second (191b) groove portions are formed along said peripheral edge (the edges of 70 and 110 as seen in gray in Figure 1 (drawn by the examiner), above) to surround a region (45) where said semiconductor element (located within region 45)(Bost et al., Col 5, Lines 5-8)) is formed.

Regarding claim 6, Figs. 18 and 19 of Bost et al., shown above, disclose the semiconductor device of claim 1, wherein said interlayer insulating film (70,110) includes first (70) and second (110) portions of different types (Oxide and BPSG)(Bost et al., Col 5, Lines 12-15, 45-47) from each other and successively formed on said main surface (see Fig. 8-10 of Bost, et al).

Regarding claim 7, Figs. 18 and 19 of Bost et al., shown above, disclose a semiconductor device comprising:

a semiconductor substrate (30) having a main surface (30a, 170);

a semiconductor element (located within region 45)(Bost et al., Col 5, Lines 5-8)) formed on said main surface (30a, 170);

an interlayer insulating film (70,110) having a top surface (110a) and a peripheral edge (the edges of 70 and 110 as seen in gray in Figure 1 (drawn by the examiner), above) extending from said top surface (110a) to said main surface (30a, 170), and formed on said main surface (30a, 170) to cover (Bost et al., Col.5, Lines 12-15) said semiconductor element (located within region 45)(Bost et al., Col 5, Lines 5-8)), wherein in said interlayer insulating film

(70,110), strip-like first (191) and second (192) groove portions are formed to be placed between said semiconductor element (located within region 45)(Bost et al., Col 5, Lines 5-8)) and said peripheral edge (the edges of 70 and 110 as seen in gray in Figure 1 (drawn by the examiner), above), to extend in parallel with said main surface (30a, 170) and to extend to cross each other at predetermined spacing (194); and

a metal (171) filling said first (191) and second (192) groove portions.

Regarding claim 8, Figs. 18 and 19 of Bost et al., shown above, disclose the semiconductor device of claim 7, wherein said first (191) and second (192) groove portions reach said main surface (30a, 170) from said top surface (110a).

Regarding claim 9, Figs. 18 and 19 of Bost et al., shown above, disclose the semiconductor device of claim 7, wherein said first (191) and second (192) groove portions are formed along said peripheral edge (the edges of 70 and 110 as seen in gray in Figure 1 (drawn by the examiner), above) to surround a region (45) where said semiconductor element (located within region 45)(Bost et al., Col 5, Lines 5-8)) is formed.

Regarding claim 10, Figs. 18 and 19 of Bost et al., shown above, disclose the semiconductor device of claim 7, wherein said interlayer insulating film (70,110) includes first (70) and second (110) portions of different types (Oxide and BPSG) (Bost et al., Col 5, Lines 12-15, 45-47) from each other and successively formed on said main surface (see Fig. 8-10 of Bost, et al).

Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Kraig whose telephone number is 571-272-0237. The examiner can normally be reached on Mon-Fri 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WFK

GEORGE ECKERT
PRIMARY EXAMINER